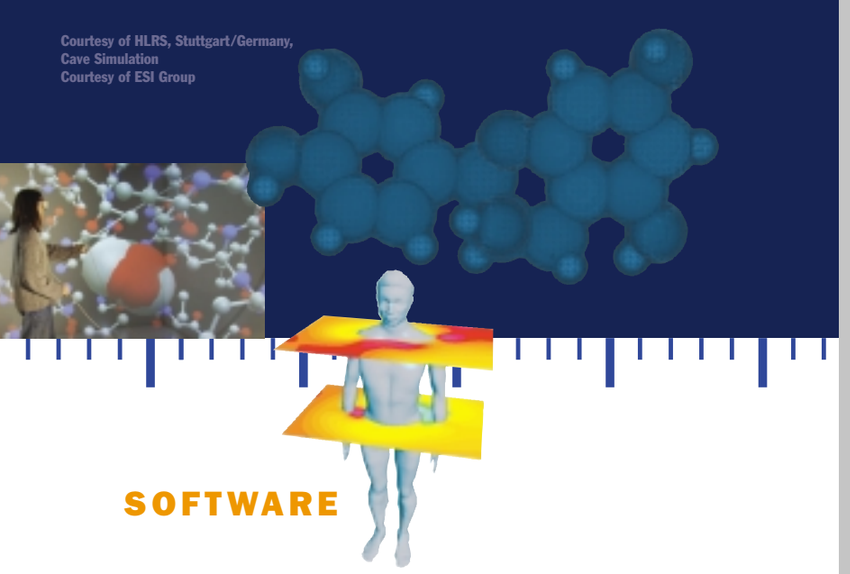

SOFTWARE

Operating System and Applications

With traditional NEC reliability and the SUPER-UX operating system, now in its 12th year, SX-6 is designed for production sites to perform production computing. All the functions other systems promise, like checkpoint-restart or a robust batch environment, are available today.

All third party applications relevant to parallel vector supercomputers are available and provide industry-leading performance. Turnaround time for solutions is minimized. Complex analysis streams can be completed overnight instead of taking the week.

Applications development is made easy through the simplicity of shared memory programming within a node, and portability is assured by industry-standard MPI and OpenMP support. NEC's PSUITE Integrated Development Environment provides all of the tools and utilities necessary under a single package for project management, editing, compiling, optimizing, and test/debugging. The cross development environment PSUITE is available on all popular workstation class products as well as Linux personal computers to maximize accessibility and development efficiency. The languages, libraries and tools available include Fortran90, OpenMP, C++, MPI and Vampir/SX.

CONFIGURATION TABLE

Selected Machine Configurations single-node Systems

Model Group Name	SX-6A					SX-6B		
Model Name	8A	7A	6A	5A	4A	4B	3B	2B
CPU								
Number of CPUs	8	7	6	5	4	4	3	2
Peak Vector Performance	64 GF	56 GF	48 GF	40 GF	32 GF	32 GF	24 GF	16 GF
Vector Registers	144 kb x 8	144 kb x 7	144 kb x 6	144 kb x 5	144 kb x 4	144 kb x 4	144 kb x 3	144 kb x 2
Scalar Registers	64 bits x 128 x 8	64 bits x 1288 x 7	64 bits x 1288 x 6	64 bits x 1288 x 5	64 bits x 1288 x 4	64 bits x 1288 x 4	64 bits x 1288 x 3	64 bits x 1288 x 2
MMU								
Memory Architecture	Shared Memory							
Capacity	32 GB/48 GB/64 GB					16 GB/24 GB/32 GB		
Peak Data Transfer Rate	256 GB/s	224 GB/s	192 GB/s	160 GB/s	128 GB/s	128 GB/s	96 GB/s	64 GB/s
Input/Output Processor								
Number of IOPs	1~4					1~2		
Max. Number of Channels	127 channels					43 channels		
Peak Data Transfer Rate	8 GB/s					4 GB/s		

SX-6

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Empowered by Innovation NEC

THE NEC SX-6

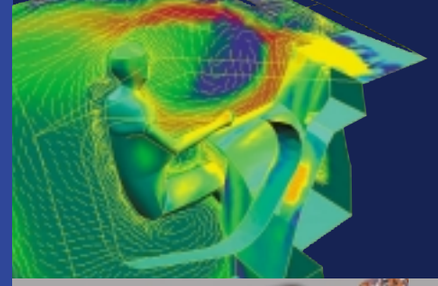
SUPERCOMPUTER WITH SINGLE-CHIP VECTOR PROCESSOR

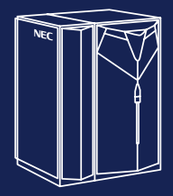
VECTOR SUPERCOMPUTING: THE STATE-OF-THE-ART

Products are turned out at an accelerating rate. Research is completed at record pace. In the time required to read this sentence each SX-6 processor performs 40 billion computations. Solutions are faster. Simulations are more exhaustive. Development is quicker. Time is precious.

Vector supercomputers have always provided the absolute highest performance available. High-performance high-bandwidth memory, powerful processors and commercial robustness for production sites. Now SX-6 breaks new ground, introducing high-end scalable parallel vector supercomputing to the technical server competitive market. With powerful shared-memory nodes and unmatched communications bandwidth it is second to none.

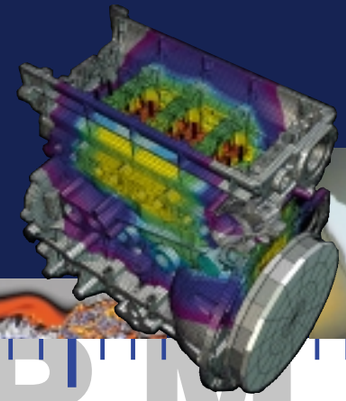
SX-6





Courtesy of ESI Group

Dr. Ulrich Rist, Institut für Aero- und Gasdynamik der Universität Stuttgart, Direct numerical Simulation of laminar-turbulent Transition in a laminar Separation Bubble



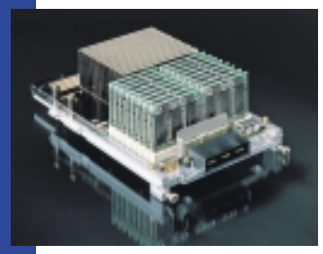
Courtesy of MSC Software
Courtesy of HLRS, Stuttgart/Germany, Cave Simulation

PERFORMANCE

HARDWARE FEATURES

Model Configuration

A SX-6 node is a complete parallel vector system consisting of 2 to 8 vector processors each with 8 GFLOPS of peak performance. The processors are coupled to an uniform shared main memory of 16 to 64 GB capacity. The SX series solution for large scalability is a hybrid system. A powerful SMP single node with uniform shared memory provides very high levels of performance for both capacity and capability requirements. For performances beyond the ones provided by a single node, a multi-node configuration having distributed memory is available. The SX-6 series is compatible with its predecessor SX-5 series. It excels in the total balance of processing performance, memory bandwidth, input/output throughput in much the same way as the former SX series systems did. Existing applications and resources can be easily migrated to the SX-6.



SX-6 Memory module

Single-node System:

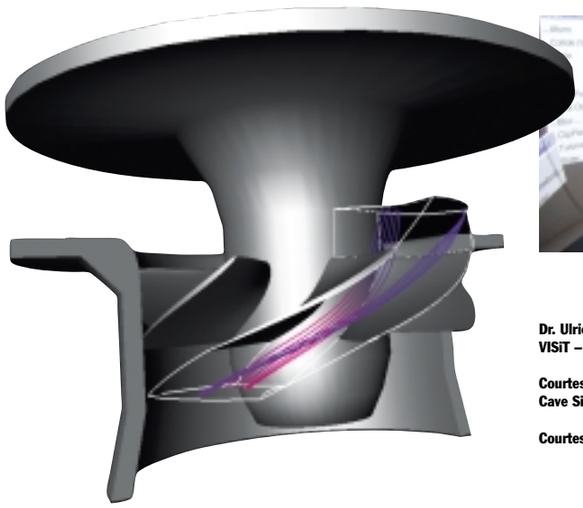
The SX-6 series single-node models scale up to 8 CPUs, delivering from 16 up to 64 GFLOPS of vector performance and offering a maximum of 64 GB main memory in shared memory architecture. A model "A" chassis can be equipped with up to 8 CPUs, a model "B" chassis can house up to 4 CPUs. The maximum I/O bandwidth is 8 GB/s for an "A" model and 4 GB/s for a model "B".

Multi-node system:

Up to 128 nodes can be connected through an Internode Crossbar Switch (IXS). SX-6 series multi-node models can be scaled up to 1024 CPUs and a peak performance of 8 TFLOPS. Although they are built on a distributed memory architecture, multi-node systems still provide a single system image. Extreme execution performance can be obtained on a wide range of applications with the powerful single node-systems connected through the ultra-high-speed crossbar system.

Ultra-high-speed Vector and Scalar Unit

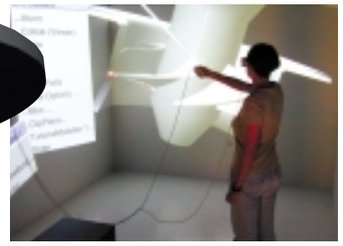
The vector unit of the SX-6 series processor consists of vector registers and 8 sets of pipelines for logical operations, multiplication, add/shift operations, division, masked operations and load/store. The scalar unit realizes ultra-high-speed scalar performance through a 4-way super scalar design. The combination of the single-chip vector microprocessor with a reduced clock cycle decreases the processing time for each instruction. This leads to the superior short vector and scalar performance.



TECHNOLOGY

The Worlds first Single-chip Vector Processor

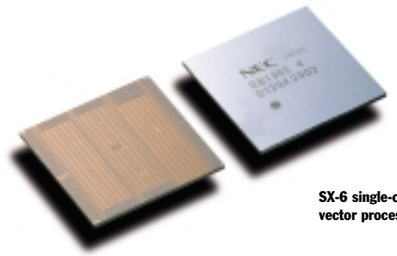
The high gate density possible for the state-of-the-art CMOS technology and LSI design enabled NEC to implement the vector processor on just one chip. This LSI and packaging technology leads to a performance of 8 GFLOPS on a single LSI. This ultrahigh integration leads to improved internal latencies and performance in comparison with former generation designs, which used dozens of chips to implement a processor, as well as highly reduced memory latencies by drastically narrowing the distance between memory and processors.



Dr. Ulrich Lang, HLRS
VISIT – Intuitive Industrial Design in Virtual Environments

Courtesy of HLRS, Stuttgart/Germany,
Cave Simulation

Courtesy of ESI, Electromagnetic simulation



SX-6 single-chip vector processor

Main Memory Unit

The SX-6 series utilizes ultra-high-speed double data rate synchronous DRAM. Single-node systems have a memory capacity of up to 64 GB and a memory bandwidth 256 GB per second. Multi-node systems have a memory capacity of up to 8 Terabytes and a maximum bandwidth of 32 Terabytes per second.

Input/Output Subsystem

The Input/Output subsystem of the SX-6 series can be configured to deliver a bandwidth of up to 8 GB per second on a single-node system. Multi-node systems scale up to an I/O capacity of 1 TB per second.

Ease of Installation

The SX-6 models' power consumption and space requirements have been reduced by 80% when compared with the previous generation of the SX series. The low power consumption allows all models to be fully air-cooled. These two elements contribute to a great reduction of installation costs and complexities.

High Reliability

The usage of highly-integrated CMOS technology has led to greatly reduced number of components in a single system. This, in turn, leads to a tremendously improved hardware reliability.